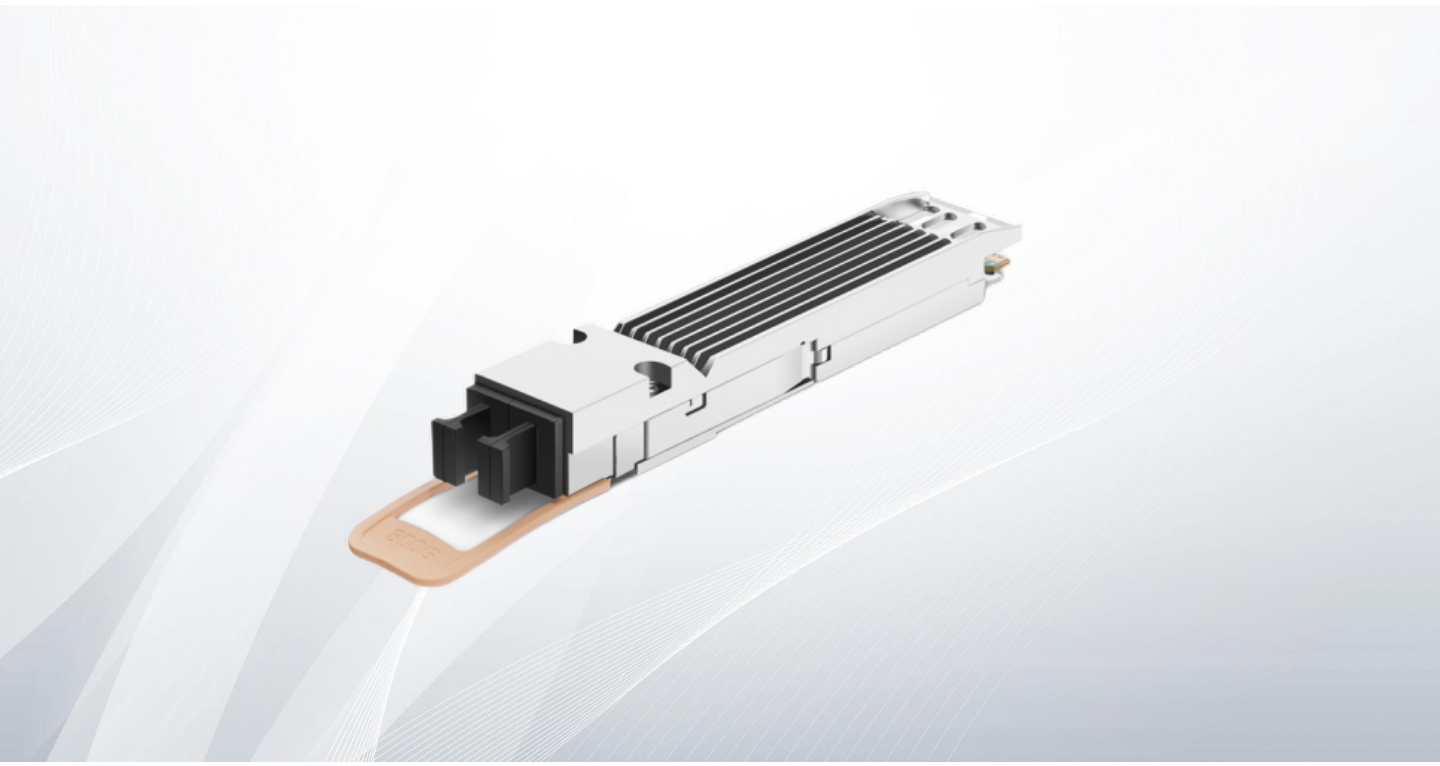
100% NVIDIA Compatible twin port transceiver, 800Gbps, 2xNDR, OSFP, 2xMPO12 APC, 850nm MMF, up to 50m, finned 5 Year Warranty

PMA4Z00-NS



Standards

- Compliant to OSFP MSA 5.0
- Compliant with CMIS 5.1
- 8x106. 25Gb/s Electrical Interface (800GAUI-8)
- Maximum Power Consumption 15W
- Single +3.3V Power Supply
- Case Temperature Range: 0 ~ +70°C
- RoHS 2.0 Complaint

Applications

- Data Centers and Cloud
- Networks

Features

- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation
- Support 800GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable
- Single +3.3V Power Supply

Description

The 800GBASE-SR8 OSFP Optical Transceiver Module is designed for use in 800Gb/s systems throughput up to 30m over OM3 or 50m over OM4multimode fiber (MMF) using a wavelength of 850nm via dual MTP/MPO-12 connectors. Digital diagnostics functions are alsoavailable via the I2C interface, as specified by the OSFP MSA, to allow access to real-time operating parameters. With these features,this easy to install, hot swappable transceiver is suitable to be used in various applications, such as data centers, high-performance computing networks, enterprise core and distribution layer applications.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{STG}	-40	85	℃
Supply Voltage	V_{CC}	0	4	V
Relative Humidity (Non-condensing)	RH	5	85	%

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Case Temperature- Operating	T_{CASE}	0	70	℃
Supply Voltage	V_{CC}	3.135	3.465	V
Power Consumption	P_{DISS}		15	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance over OM3		0.5	30	M
Link Distance over OM4		0.5	50	M

III. Optical Characteristics

Parameter	Min.	Typical	Max.	Unit
Transmitter				
Signaling Rate, Each Lane		53.125 ± 100 ppm		GBd
Lane Wavelength Range		850		nm
RMS Spectral Width			0.6	nm
Modulation Format		PAM4		
Average Optical Power Per Lane	-4.6		4	dBm
Outer Optical Modulation Amplitude (OMAouter), Each Lane				
for TDECQ≤1.8dB	-2.6		3.5	dBm
for 1.8<TDECQ≤4.4dB	-4.4+TDECQ		3.5	dBm
Outer Optical Modulation Amplitude (OMAouter), Each Lane				
for TECQ≤1.8dB	-2.6		3.5	dBm
for 1.8<TECQ≤4.4dB	-4.4+TECQ		3.5	dBm
Transmitter and Dispersion Eye Closure for PAM4, Each Lane			4.4	dB
Transmitter Eye Closure for PAM4 (TECQ), Each Lane			4.4	dB
ExtinctionRatio	2.5			dB
Transmitter Excursion, Each Lane			2	dB
Transmitter Transition Time, Each Lane			17	ps

Parameter	Min.	Typical	Max.	Unit
Average Launch Power Per Lane @ TX Off State			-30	dBm
Relative Intensity Noise12 (OMA)			-131	dB/Hz
Optical Return Loss Tolerance			12	dB
Encircled Flux		>=86% at 19μm <=30% at 4.5μm		dB
Receiver				
Signaling Rate Each Lane		53.125±100ppm		GBd
Lane Wavelength Range		850		nm
Modulation Format		PAM4		
Damage Threshold	5			dBm
Average Receive Power, Each Lane	-6.4		4	dBm
Receiver Power, Each Lane (OMA)			3.5	dBm
Receiver Sensitivity Each Lane (OMAouter)				
for TECQ≤1.8dB			-4.6	dBm
for 1.8<TECQ≤4.4dB			-6.4+TECQ	dBm
Receiver Reflectance			-12	dB
Stressed Receiver Sensitivity (OMAouter), Each Lane			-2	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		4.4		dB

Parameter	Min.	Typical	Max.	Unit
OMAouter of Each Aggressor Lane		3.5		dBm

IV. High Speed Electrical Signals

Parameter	Min.	Typ.	Max.	Unit
Transmitter Electrical Input Characteristics at TP1				
Signaling Rate, Per Lane		53.125		GBd
Differential Pk-pk Input Voltage Tolerance	900			mV
Common-mode to Differential Return Loss	802.3ck Equation(120G-1)			
Effective Return Loss	TBD			
Differential Termination Mismatch			10	%
Module Stressed Input Test		See 120G.3.4.1		
Single-ended Voltage Tolerance Range	-0.4		3.3	V
DC Common-mode Voltage	-350		2850	mV
Receiver Electrical Output Characteristics at TP4				
Signaling Rate Per Lane		53.125		GBd
AC common-mode Output Voltage(RMS)			17.5	mV
Differential Peak-to-peak Output Voltage			900	dB
Near-end ESMW (Eye Symmetry Mask Width)		TBD		UI
Near-end Eyeheight, Differential	24			mV

Parameter	Min.	Typ.	Max.	Unit
Near-end Vertical Eye Closure			7.5	dB
Far-end ESMW (Eye Symmetry Mask Width)		TBD		UI
Far-end Eyeheight, Differential	24			mV
Far-end Vertical Eye Closure			7.5	dB
Far-end Pre-cursor ISI Ratio		TBD		UI
Common Mode to Differential Conversion Return Loss		802.3ck 120G-1		dB
Effective Return Loss	TBD			dB
Differential Termination Mismatch			10	%
Transition Time (min,20%to80%)		TBD		ps
DC Common Mode Voltage	-350		2850	mV

V. Low Speed Electrical Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for Fast Mode, 20mA for Fast-mode Plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	

Parameter	Symbol	Min.	Max.	Unit	Condition
Total Bus Cpacitive Load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up Resistor, Max
			200	pF	1.6k Ohms Pull up Resistor, Max
LPMode/TxDis, Reset and ModeSelL	VIL	-0.3	0.8	V	|Iin| </= 125uA for Vin < V_{CC}
	VIH	2	Vcc+0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	V_{CC}-0.5	V_{CC}+0.3	V	10k Ohms Pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can be implemented as a short-circuit to GND on the module

VI. Pin Definition

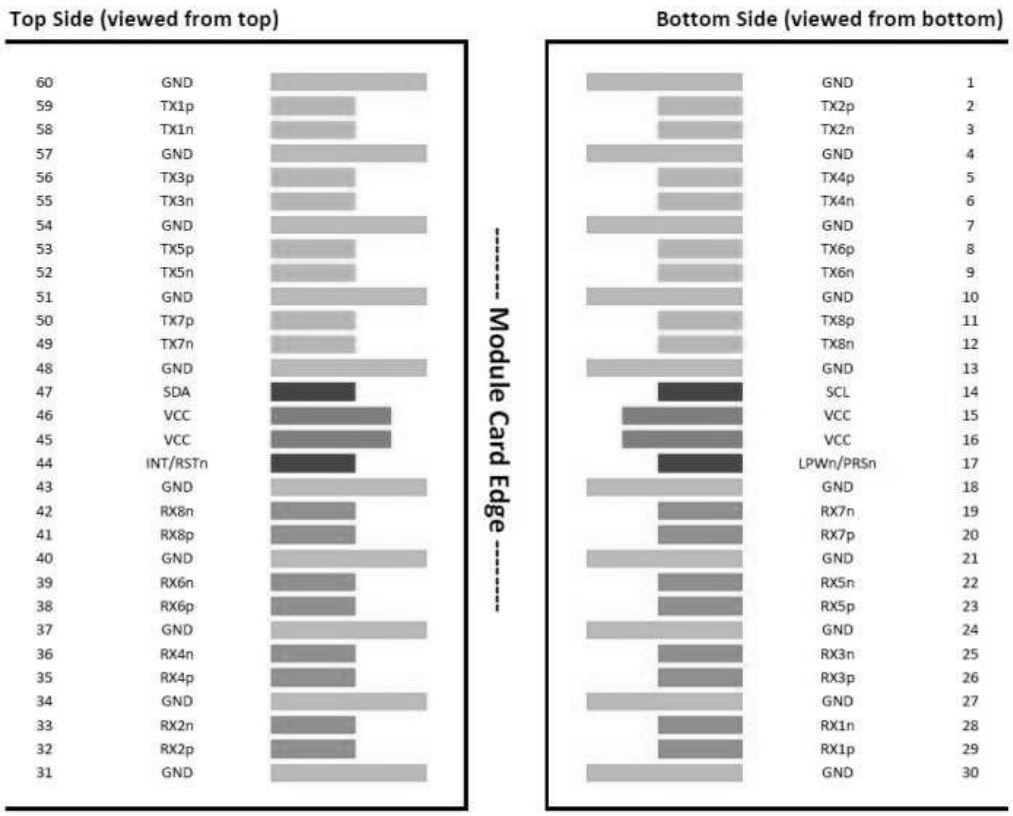


Figure1. OSFP800 800G Contact Assignment

VII. Pin Description

Pin	Symbol	Logic	Description	Note
1	GND		Ground	
2	T_X2p	CML-I	Transmitted Data Non-Inverted	
3	T_X2n	CML-I	Transmitted Data Inverted	
4	GND		Ground	
5	T_X4p	CML-I	Transmitted Data Non-Inverted	
6	T_X4n	CML-I	Transmitted Data Inverted	

Pin	Symbol	Logic	Description	Note
7	GND		Ground	
8	T_x6p	CML-I	Transmitted Data Non-Inverted	
9	T_x6n	CML-I	Transmitted Data Inverted	
10	GND		Ground	
11	T_x8p	CML-I	Transmitted Data Non-Inverted	
12	T_x8n	CML-I	Transmitted Data Inverted	
13	GND		Ground	
14	SCL	LVCMOS-I/O	2-wire Serial Interface Clock	1
15	VCC		+3.3V Power	
16	VCC		+3.3V Power	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	2
18	GND		Ground	
19	R_x7n	CML-O	Receiver Data Inverted	
20	R_x7p	CML-O	Receiver Data Non-Inverted	
21	GND		Ground	
22	R_x5n	CML-O	Receiver Data Inverted	
23	R_x5p	CML-O	Receiver Data Non-Inverted	
24	GND		Ground	

Pin	Symbol	Logic	Description	Note
25	R_X3n	CML-O	Receiver Data Inverted	
26	R_X3p	CML-O	Receiver Data Non-Inverted	
27	GND		Ground	
28	R_X1n	CML-O	Receiver Data Inverted	
29	R_X1p	CML-O	Receiver Data Non-Inverted	
30	GND		Ground	
31	GND		Ground	
32	R_X2p	CML-O	Receiver Data Non-Inverted	
33	R_X2n	CML-O	Receiver Data Inverted	
34	GND		Ground	
35	R_X4p	CML-O	Receiver Data Non-Inverted	
36	R_X4n	CML-O	Receiver Data Inverted	
37	GND		Ground	
38	R_X6p	CML-O	Receiver Data Non-Inverted	
39	R_X6n	CML-O	Receiver Data Inverted	
40	GND		Ground	
41	R_X8p	CML-O	Receiver Data Non-Inverted	
42	R_X8n	CML-O	Receiver Data Inverted	

Pin	Symbol	Logic	Description	Note
43	GND		Ground	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	2
45	VCC		+3.3V Power	
46	VCC		+3.3V Power	
47	SDA	LVCMOS-I/O	2-wire Serial Interface Clock	1
48	GND		Ground	
49	T_X7n	CML-I	Transmitted Data Inverted	
50	T_X7p	CML-I	Transmitted Data Non-Inverted	
51		GND	Ground	
52	T_X5n	CML-I	Transmitted Data Inverted	
53	T_X5p	CML-I	Transmitted Data Non-Inverted	
54		GND	Ground	
55	T_X3n	CML-I	Transmitted Data Inverted	
56	T_X3p	CML-I	Transmitted Data Non-Inverted	
57		GND	Ground	
58	T_X1n	CML-I	Transmitted Data Inverted	
59	T_X1p	CML-I	Transmitted Data Non-Inverted	
60		GND	Ground	

Notes:

1. Open-Drain with pull up resistor on Host.
2. See pin description for required circuit.

VIII. Principle Diagram

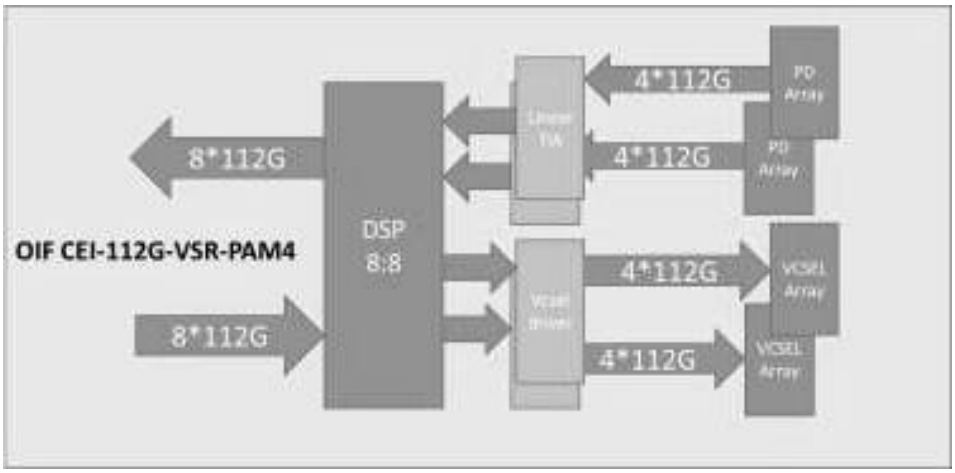


Figure 2. Module Block Diagram

IX. Digital Diagnostic Monitoring Specifications

Parameter	Specification	Unit
Temperature Monitor Absolute Error	±3	℃
Supply Voltage Monitor Absolute Error	±5	%
I_Bias Monitor Absolute Error	±10	%
Received Power (Rx) Monitor Absolute Error	±3.0	dB
Transmit Power (Tx) Monitor Absolute Error	±3.0	dB

X. Mechanical Dimensions

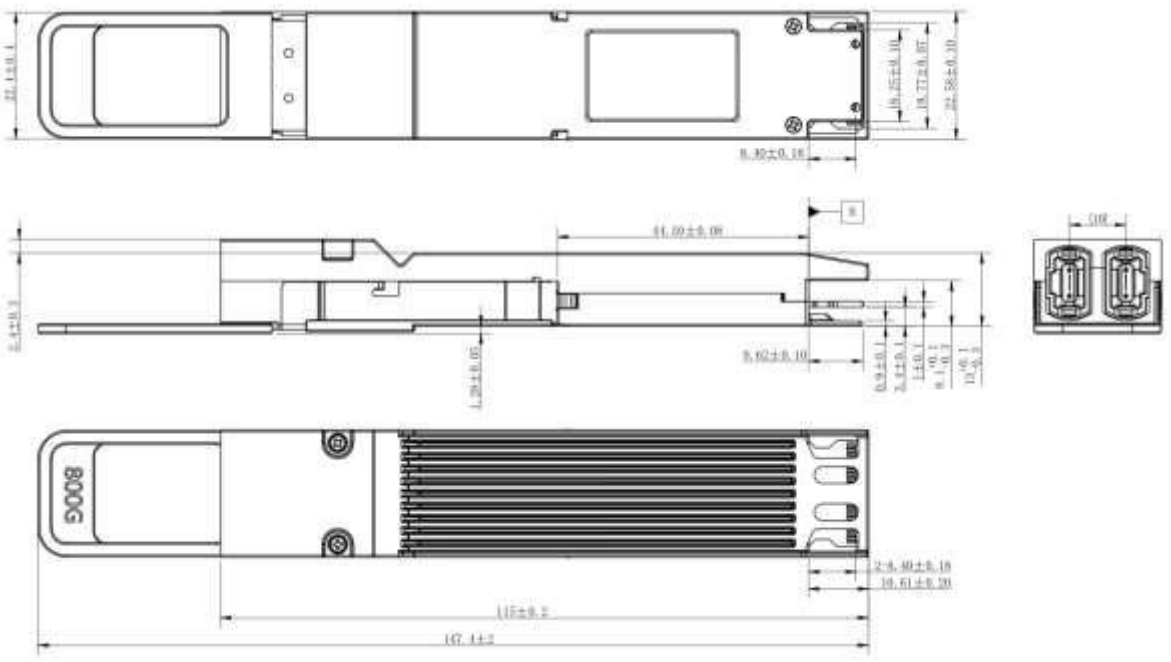


Figure 3. Mechanical Dimensions

Order Information

Part Number	Description
PMA4Z00-NS	100% NVIDIA Compatible twin port transceiver, 800Gbps, 2xNDR, OSFP, 2xMPO12 APC, 850nm MMF, up to 50m, finned 5 Year Warranty

Questions? Contact **GOPNY@PNY.COM**

PNY Technologies, Inc. 100 Jefferson Road, Parsippany, NJ 07054 | Tel 973-515-9700 | Fax 973-560-5590 | www.PNY.com