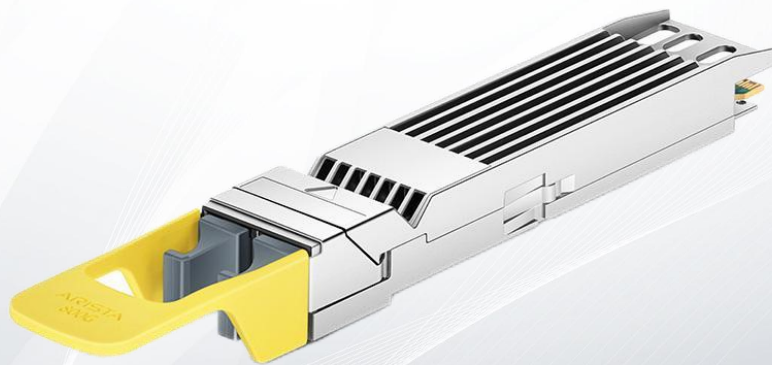


# 100% NVIDIA Compatible twin port transceiver, 800Gbps, 2xNDR, OSFP, 2xMPO, 1310nm SMF, up to 500m, finned 5 Year Warranty

PMS4X00-NM



## Application

- 800G InfiniBand
- 2x 400GBASE-DR4
- Cloud Networks

## Features

- Compliant with IEEE 802.3cu-2021: - 2x400GBASE-DR4 optical interface
- Compliant with IEEE P802.3ck D2.2 - 2x400GAUI-4 C2M electrical interface
- Compliant with OSFP MSA HW Rev 4.1 Type 2 housing with Dual MPO-12 connector
- Compliant with CMIS Rev 5.0
- Maximum Power Consumption 16.5W
- Operating Temperature Range: 0°C ~ +70 °C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

## Description

The PNY for Mellanox MMS4X00-NM Compatible OSFP Optical Transceiver Module is designed for 800GBASE throughput up to 500m over single-mode fiber (SMF) with dual MTP/MPO-12 connectors. The OSFP-DR8-800G module can convert 8-channel 106.25Gb/s electrical data to 8-channel 106.25Gb/s optical signals. Similarly, it optically converts 8-channel 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The OSFP-DR8-800G Optical Transceiver is a high performance, cost effective module for optical data communication applications supporting 800G InfiniBand.

## Product Specifications

### I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
<b>Storage Temperature Range</b>	TS	-40	85	°C	
<b>Supply Voltage</b>	V <sub>CC</sub>	-0.5	3.6	V	
<b>Relative Humidity (non-condensing)</b>	RH	5	95	%	
<b>Data Input Voltage Differential</b>	V <sub>DIP</sub> -V <sub>DIN</sub>		1	V	
<b>Control Input Voltage</b>	VI	-0.3	V <sub>CC</sub> +0.5	V	
<b>Control Output Current</b>	I <sub>O</sub>	-20	20	mA	

### II. Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Operating Case Temperature</b>	T <sub>OPR</sub>	0		70	°C	1
<b>Power Supply Voltage</b>	V <sub>CC</sub>	3.135	3.3	3.465	V	
<b>Instantaneous peak current at hot plug</b>	I <sub>CC_IP</sub>				mA	
<b>Sustained peak current at hot plug</b>	I <sub>CC_SP</sub>				mA	
<b>Maximum Power Dissipation</b>	P <sub>D</sub>			16.5	W	

<b>Maximum Power Dissipation, Low Power Mode</b>	$P_{DLP}$				W	
<b>Signalling Speed per Lane</b>	DRL		53.125		GBd	
<b>Control Input Voltage High</b>	$V_{IH}$	$V_{CC} * 0.7$		$V_{CC} + 0.3$	V	
<b>Control Input Voltage Low</b>	$V_{IL}$	-0.3		$V_{CC} * 0.3$	V	
<b>Two Wire Serial Interface Clock Rate</b>				400	kHz	
<b>Power Supply Noise 1 kHz - 1 MHz (p-p)</b>				66	mVpp	
<b>Operating Distance</b>		2		500	m	

### III. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Wavelength</b>	$\lambda_C$	1304.5	1311	1317.5	nm	

#### Transmitter (per Lane)

<b>Side Mode Suppression Ratio</b>	SMSR	30			dB	
<b>Average Launch Power, each lane</b>	$AOP_L$	-2.9		4.0	dBm	1
<b>Outer Optical Modulation Amplitude (OMA<sub>outer</sub>), each Lane</b>	$T_{OMA}$	-0.8		4.2	dBm	
<b>Launch Power in OMA<sub>outer</sub> minus TDECQ, each lane</b>	$T_{OMA-TDECQ}$	-2.2			dBm	
<b>Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane</b>	TDECQ			3.4	dB	
<b>Average Launch Power of OFF Transmitter, each lane</b>	$T_{OFF}$			-15	dBm	
<b>Extinction Ratio</b>	ER	3.5			dB	
<b>Transmitter transition time (max)</b>	$T_r$			17	ps	

<b>RIN21.4OMA (max)</b>	RIN			-136	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL			21.4	dB	
<b>Transmitter Reflectance</b>	$T_R$			-26	dB	2

#### Receiver (Per lane)

<b>Wavelength L0</b>	$\lambda_{CO}$	1304.5	1311	1317.5	nm	
<b>Damage Threshold, each Lane</b>	$AOP_D$	5			dBm	
<b>Average Receive Power, each Lane</b>	$AOP_R$	-5.9		4	dBm	
<b>Receive Power (OMAouter), each Lane</b>	$OMA_R$			4.2	dBm	
<b>Receiver Reflectance</b>	RR			-26	dB	
<b>Receiver Sensitivity (OMAouter), each Lane</b>	$S_{OMA}$			Max(-3.9, SECQ - 5.3)	dBm	3
<b>Stressed Receiver Sensitivity (OMAouter), each Lane</b>	SRS			-1.9	dBm	4

#### Conditions of stressed receiver sensitivity test

<b>Stressed eye closure for PAM4 (SECQ), lane under test</b>	SECQ		3.4		dB	
<b>OMAouter of each aggressor lane</b>			4.2			

#### Notes:

- 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength
- 2: Transmitter reflectance is defined looking into the transmitter
- 3: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
- 4: Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$

#### IV. Electrical Characteristics(compliant with IEEE P802.3ck C2M))

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Transmitter (per Lane)</b>						
<b>AC common-mode output Voltage (RMS)</b>				25	mV	
<b>Differential peak-to-peak output voltage</b>				600	mV	
<b>Short mode</b>				900	mV	
<b>Long mode</b>						
<b>Eye height, differential</b>	EH	15			mV	
<b>Vertical eye closure</b>	VEC			12	dB	
<b>Common-mode to differential return loss</b>	RLDc		802.3ck 120G-1		dB	
<b>Effective return loss, ERL</b>	ERL	8.5			dB	
<b>Differential termination mismatch</b>				10	%	
<b>Transition time (20% to 80%)</b>		8.5			ps	
<b>Receiver (per Lane)</b>						
<b>Differential pk-pk input Voltage tolerance</b>		900			mV	
<b>AC common-mode RMS voltage tolerance (TP1a)</b>		25			mV	
<b>Differential to common-mode return loss</b>	RLcd		802.3ck 120G-2		dB	
<b>Effective return loss, ERL</b>	ERL	8.5			dB	
<b>Differential termination mismatch</b>				10	%	
<b>Single-ended voltage tolerance range</b>		-0.4		3.3	V	
<b>DC common-mode Voltage</b>		-0.35		2.85	V	

### V. Electrical Specification Low Speed Signal

Parameter	Symbol	Min	Max	Unit	Condition
<b>Module output SCL and SDA</b>	$V_{OL}$	0	0.4	V	
<b>Module Input SCL and SDA</b>	$V_{IL}$	-0.3	$V_{CC} * 0.3$	V	
	$V_{IH}$	$V_{CC} * 0.7$	$V_{CC} + 0.5$	V	
<b>LPMode/TxDis, ResetL and ModSelL</b>	$V_{IL}$	-0.3	0.8	V	
	$V_{IH}$	2	$V_{CC} + 0.3$	V	
<b>IntL/RxLos</b>	$V_{OL}$	0	0.4	V	
	$V_{OH}$	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	

### VI. Pin Definitions

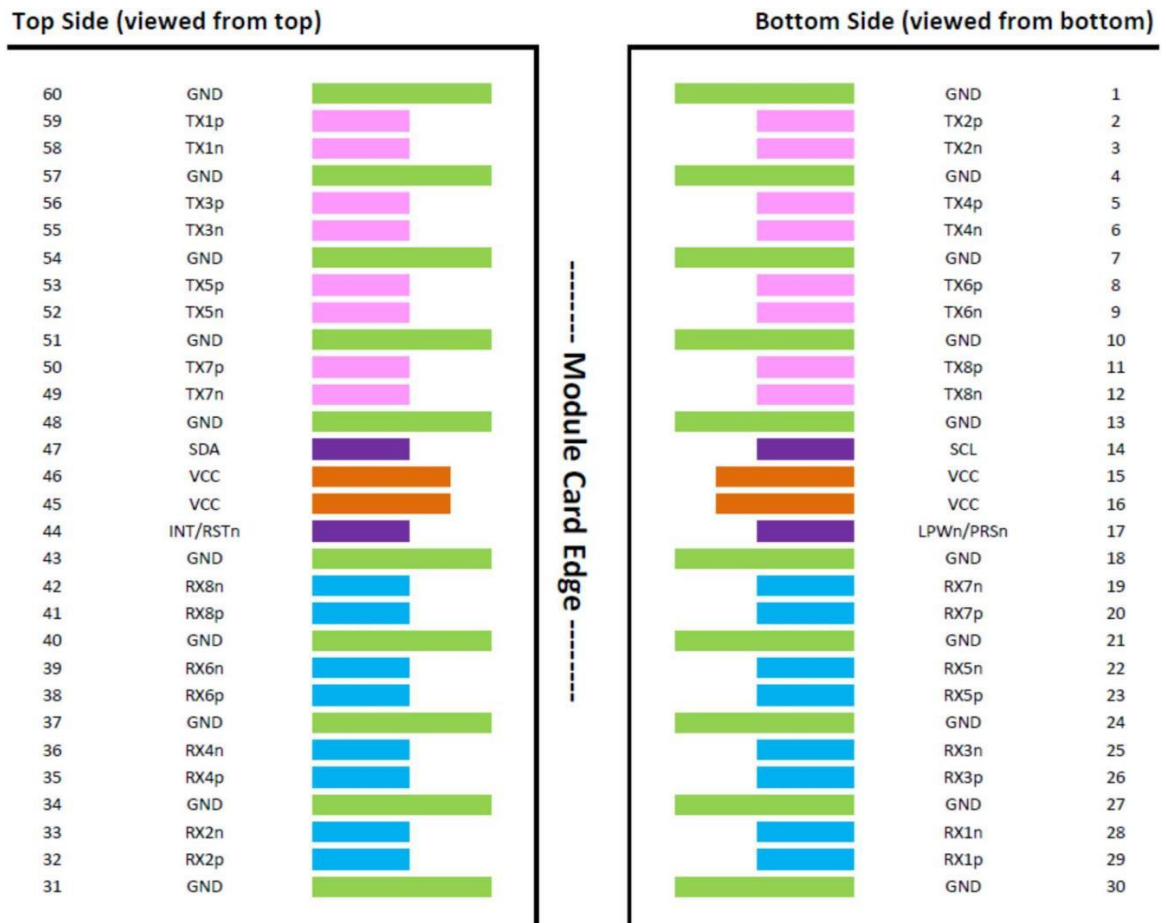


Figure 1 – Pinout definitions of OSFP module inputs/outputs

## VII. Pin Definitions

PIN	Symbol	Description	Logic	Note
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/PRS <sub>n</sub>	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	
20	RX7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		

22	RX5n	Receiver Data Inverted	CML-O	
23	RX5p	Receiver Data Non-Inverted	CML-O	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	
26	RX3p	Receiver Data Non-Inverted	CML-O	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	
29	RX1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	
33	RX2n	Receiver Data Inverted	CML-O	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	
36	RX4n	Receiver Data Inverted	CML-O	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	
39	RX6n	Receiver Data Inverted	CML-O	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	
42	RX8n	Receiver Data Inverted	CML-O	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2-wire Serial interface data	LVCM OS-I/O	
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	
50	TX7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	
53	TX5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		



55	TX3n	Transmitter Data Inverted	CML-I
56	TX3p	Transmitter Data Non-Inverted	CML-I
57	GND	Ground	
58	TX1n	Transmitter Data Inverted	CML-I
59	TX1p	Transmitter Data Non-Inverted	CML-I
60	GND	Ground	

### VIII. Recommended OSFP Host Board Schematic

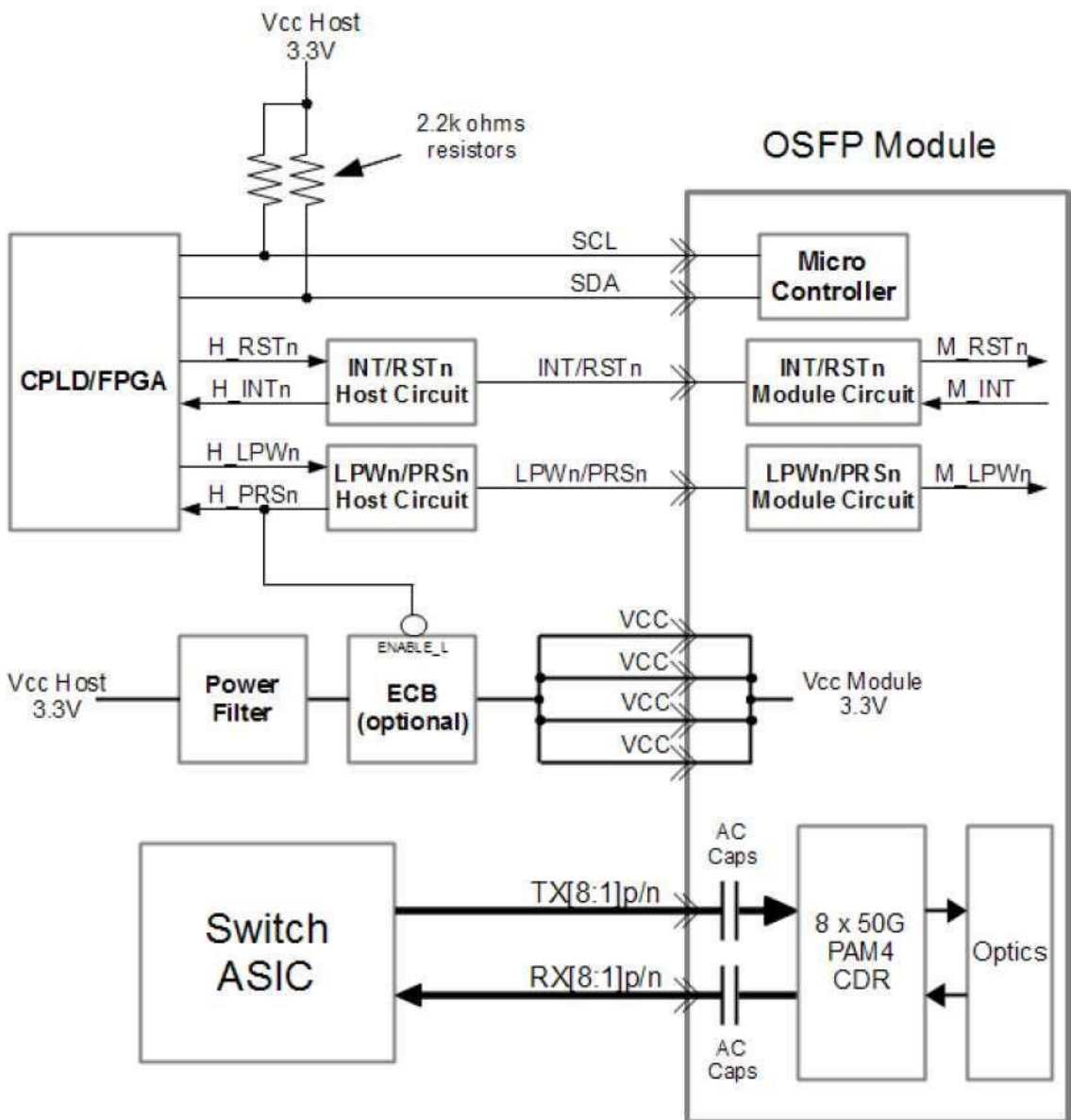
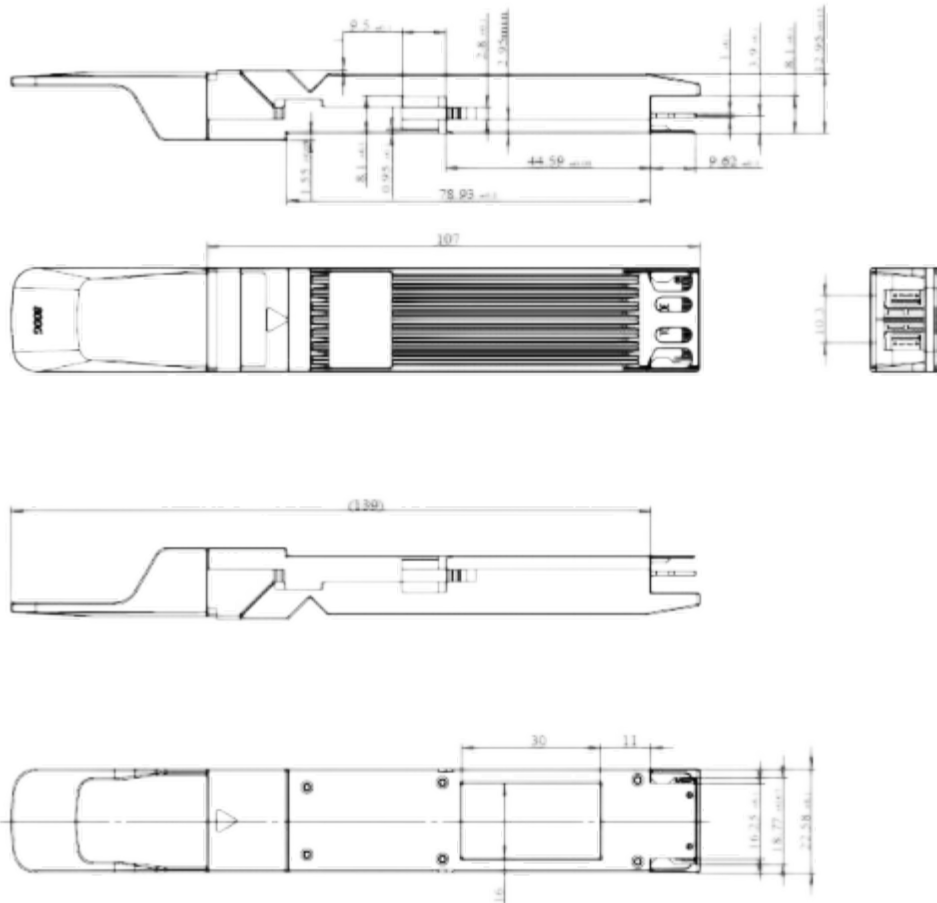


Figure 2. Recommended OSFP Host Board Schematic

### IX. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V <sub>CC</sub>	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.8 to +5.3	±3	dB	Internal
Rx Receive Power (Each Lane)	-9.1 to +5.3	±3	dB	Internal

### X. Mechanical Diagram



## Ordering Information

Part Number	Description
PMS4X00-NM	100% NVIDIA Compatible twin port transceiver, 800Gbps, 2xNDR, OSFP, 2xMPO, 1310nm SMF, up to 500m, finned 5 Year Warranty

Questions? Contact [GOPNY@PNY.COM](mailto:GOPNY@PNY.COM)